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09/864561

Express Mail Label No. Dated: _____

Docket No.: 08211/000S081-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Hee Wong

Patent No.: 6,873,318

Issued: March 29, 2005

For: METHOD AND APPARATUS FOR ADDRESSING BEAT PATTERNS IN AN INTEGRATED VIDEO DISPLAY SYSTEM

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

MS Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several errors which should be corrected.

In the Specification:

First Page Col. 2 (Abstract), Line 9 Delete "flips-flops" and insert --flip-flops--.

Column 1, Line 42, Delete "interfacing" and insert -- interfering --.

Column 1, Line 42, Delete "ether" and insert -- either --.

Column 2, Line 2, Delete "Afterwords" and insert -- Afterwards --.

Column 2, Line 5, Delete "embodiments" and insert -- embodiment --.

Column 3, Line 25, Delete "<100" and insert - - >100 - -.

Column 3, Line 33, "clocks" and insert - - clock - -.

Column 4, Line 8, Delete "syn" and insert - - sync - -.

Column 4, Line 61, Delete "selected" and insert - - select - -.

Column 5, Line 27, Delete "pixels" and insert - - pixel - -.

Column 5, Line 32, Delete "resynchronization" and insert - - re-synchronization - -.

Column 5, Line 34, Delete "fine" and insert - - finer - -.

Column 5, Line 47, Delete "211" and insert - - 221 - -.

Column 6, Line 3, After "from" delete "the".

Column 6, Line 25, In Claim 1, after "signal" delete "data first stage " and insert - - at a final stage - -.

Column 6, Line 32, In Claim 3, after "video" delete "signal".

Column 6, Line 45, In Claim 7, delete "integral" and insert - - integrated - -,

Column 6, Line 55, In Claim 7, insert -- the -- before "re-clocking".

Column 6, Line 55, In Claim 7, delete "on figured" and insert -- configured --.

Column 7, Line 22, In Claim 12, after "interfering" delete "the".

Column 8, Line 17, In Claim 17, delete "blocked" and insert -- clocked --.

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of the Specification and Amendments to the Claims.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: June , 2005

Respectfully submitted,

By _____

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PTO/SB/44 (04-05)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,873,318
APPLICATION NO.	:	09/864,561
ISSUE DATE	:	March 29, 2005
INVENTOR(S)	:	Hee Wong

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

First Page Col. 2 (Abstract), Line 9 Delete "flips-flops" and insert --flip-flops--.

Column 1, Line 42, Delete "interfacing" and insert -- interfering --.

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Column 5, Line 34, Delete "fine" and insert - - finer - -.

Column 5, Line 47, Delete "211" and insert - - 221 - -.

Column 6, Line 3, After "from" delete "the".

Column 6, Line 25, In Claim 1, after "signal" delete "data first stage " and insert - - at a final stage - -.

Column 6, Line 32, In Claim 3, after "video" delete "signal".

Column 6, Line 45, In Claim 7, delete "integral" and insert - - integrated - -,

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(Also Form PTO-1050)

Column 6, Line 55, In Claim 7, insert -- the -- before "re-clocking".

Column 6, Line 55, In Claim 7, delete "on figured" and insert -- configured --.

Column 7, Line 22, In Claim 12, after "interfering" delete "the".

Column 8, Line 17, In Claim 17, delete "blocked" and insert -- clocked --.

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Docket No. 50019.54US01/P04766

METHOD AND APPARATUS FOR ADDRESSING BEAT PATTERNS IN AN INTEGRATED VIDEO DISPLAY SYSTEM

Field of the Invention

The present invention relates to the field of digital circuits, and in particular, to integrated video display circuits.

Background of the Invention

Many video display systems show beat patterns when the video data contains specific display patterns. These beat patterns show up on a display as bands, streaks, or other forms. The beat pattern frequencies are not normally an integer multiple of half of the video horizontal scanning frequency, and hence the beat patterns tend to manifest themselves as moving patterns. Until now, it has not been known exactly what caused the beat patterns, and very little was known about how to eliminate them.

Existing attempts to address beat patterns typically seek to alter or tune the frequencies of the particular subsystems to minimize the symptoms of the beat patterns. For instance, one method sometimes used is to force the frequency of the beat pattern to some relationship of the horizontal and vertical scanning frequencies so that the pattern is non-moving. This method does not eliminate the beat pattern but rather hides it from the human eye. This method takes advantage of the fact that the human eye cannot easily detect non-moving objects, especially objects with fuzzy outlines. However, even if the beat pattern is not moving and nearly invisible to the human eye, the diminished video quality is still present.

Another method sometimes used is the canceling method. With this method, inverted beat pattern attributes (such as intensity) are introduced on consecutive horizontal scan lines so the pattern seems to "cancel out" its appearance.

Still another method sometimes used is the resizing method. With this method, one or more of the system frequencies is changed such that the physical size of the interfering bands is either very small or very large to the viewer. If the beat

frequency were set to a much higher frequency than the horizontal scanning frequency, then the "bands" would become tiny, and hence less visible to the viewer. Similarly, if the beat frequency were set sufficiently low (e.g., 0Hz), then only one band with uniform intensity would appear on the screen. From the viewer's perspective, the interfering patterns would no longer exist

Yet another method sometimes used is the blurring method. This technique involves sweeping one or more of the system frequencies in a pseudo random manner. This technique results in a blurred beat pattern which is less visible to the viewer.

Unfortunately, these existing attempts to solve the beat pattern problem are inadequate because they do not address the problem but rather only try to mask its symptoms. The result of each of these methods is merely a beat pattern which may be less visible to the viewer, but which still results in diminished video quality. Accordingly, both the actual problem causing beat patterns and an acceptable solution to that problem have eluded those skilled in the art.

Summary of the Invention

The present invention overcomes the problems identified above by identifying that beat patterns are the modulation results of one or more interfering frequencies mixing with the video pixel frequency in a video display system. To address the problem, a method of "Cleaning-up Afterwards" is used. Using a "clean" local pixel clock to re-clock the final stage of the video data path to the RGB DACs eliminates the beat patterns. In one embodiment, re-clocking flip-flops are used to re-time a video data signal feeding a video Red/Green/Blue Digital-to-Analog converters (RGB DACs) such that data edge jitters due to interference are removed. The resulting picture quality is free of beat patterns. This method also allows more design freedom, such as higher jitter tolerance budget for the entire clock distribution system and increased distance between the video data source and the RGB DACs.

A more complete appreciation of the present invention and its improvements can be obtained by reference to the accompanying drawings, which are

subsystem blocks and each block may use a different clock frequency. Due to implementation constraints, clock interferences from nearby blocks are unavoidable. In a video display sub-system, these interferences alter slightly the width of the pulse created by the video pixel clock, which produces beat patterns.

The inventors have determined that one display mode suffering from the problem is the 1280x1024x75Hz mode in certain video display systems. When the video data stream contains a "1010" pattern, its frequency beats with the second harmonic frequency of a 33 MHz PCI clock signal (66MHz), thereby producing beat patterns. The "1010" pattern should only show stable fine vertical lines on the display screen without any beat patterns. These lines and the gaps between them are so fine that the viewer should see a half intensity solid color display. However, the beat components change the intensity of some displayed regions causing bands appear. The combined effect of the RGB video outputs also changes the color hue of these bands. If the beat frequency has a non-integer relationship with half of the horizontal scanning frequency, then the bands move. Adjusting the frequency relationship can change the direction of the movement. The intensity difference between the bright and the dim levels of the band patterns can be as small as a couple percent. This intensity difference is caused by width modulation of the "1010" video data pulses. Although the magnitude is minor, it degrades the video quality significantly. The "1010" video pulses should have a typical pulse width of 7.4nSec (135MHz pixel frequency). A width modulation of ±100pSec produces noticeable bands to the viewer. Within the time duration of a band, all pulse widths are modulated in one direction, either positively or negatively. If the beat frequency is much lower than the pixel frequency, then there are many (e.g., > 100) consecutive pulses modulated in that direction.

What the inventors found is that in many video circuit designs, the clock signal driving the video RGB Digital-to-Analog Converters (DACs) requires many buffers and connecting wires from the clock source to the destination DACs. This long signal path can possibly pick up unwanted interferences from nearby subsystems. The unwanted interferences can change slicing levels of the clock buffers, which causes non-uniform clock periods. This distorted clock driving the DAC produces width modulated video pulses. The interferences are sometimes coupled through the supply

and ground connections. Moreover, the DAC switching circuit also contributes to the pulse width modulation. As mentioned previously, a minor ±100pSec clock modulation results in noticeable bands to the viewer. In practice, a small amplitude of ±100mV interfering signal adding to the clock input node produces a similar effect. The external clock input must slew faster than 1 nSec/Volt otherwise the bands would be even more noticeable (more than ±100pSec pulse width modulation). The problem has been seen when the interfering signal is either a square or sine wave.

After making this determination, the inventors solved the problem by using a "clean" local pixel clock to re-clock the final stage of the video data path to the RGB DACs. By re-clocking the video data at the final stage, the interfering influence of other system clocks is removed, resulting in a beat-pattern free data signal. The final stage can be an integral design of the video DACs. This solution also allows more design freedom, such as higher jitter tolerance budget for the entire clock distribution system and increased distance between the video data source and the RGB DACs. This implies a remote connection between the video data source and the DACs.

Illustrative Re-Clocking Circuit

One embodiment of the invention employs re-clocking flip-flops to re-time the input signals feeding the video Red/Green/Blue Digital-to-Analog converters (RGB DACs) such that data edge jitters due to interference are removed. This scheme addresses the problem directly, and the resulting picture quality is free of beat patterns.

FIGURE 1 illustrates a schematic diagram of an electronic circuit 100 for connecting a video data source 103 to a video DAC circuit 105. An external clock reference 107 provides a signal to a local clock generator 109, which in turn outputs a pixel clock signal 111 via a clock buffer 113. Clock logic circuitry 115 processes the pixel clock signal 111 and provides a processed pixel clock signal 117 to the video DAC circuit 105 as well as a video data source 119. The video data source 119 provides a video data signal 121 to the video DAC circuit 105 in sync with the processed pixel clock 117.

The video data source 103 can be either remote or local to the video DAC circuit 105. The pixel clock signal 111 and the processed pixel clock signal 117 are sensitive paths to interferences. If there are more circuitries extending these signal

DAC 129 is taken from the local clock generator 109. Because the connection is short and local, interference from other system clock sources should be an insignificant cause of beat patterns. The second flip-flop 127, which again may contain several flip-flops, is re-clocked with the local "clean" timing, thus the output should be free of beat patterns.

The third operation mode (Scheme C) occurs when the scheme select switch 123 is in the "C" position. In that position, the processed pixel clock 117 is coupled to the D input of a third flip-flop 133, the Q output of which is coupled to the clock inputs of the second flip-flop 127 and the RGB DAC 129. However, the clock input of the third flip-flop 133 is fed by a clock signal 135 from the clock phase selector 131. In this configuration, the processed pixel clock 117 is used to latch the video data signal 121 into the first flip-flop 125, but the local clock generator 109 is used for timing the second flip-flop 127 and the DAC 129.

Scheme C is applicable to specific designs where the processed pixel clock signal 117 is not a buffered version (e.g., not the same frequency) of the pixel clock signal 111. For some designs and under some video modes, there are some circuit functions, such as a divide-by-2 function, employed between the pixel clock signal 111 and the processed pixel clock signal 117. These types of circuits cannot use Scheme B for re-clocking because the clock frequencies are different. Hence, Scheme C employs an additional D-flip-flop 133 which takes a different (e.g., 2x) frequency clock from the local clock generator to re-time the edges of the processed pixel clock signal 117. The output of the third flip-flop 133 is then used to perform the normal re-clocking function as described in Scheme B.

The clock phase selector 131 selects the proper clock phase for its two clock outputs so that the appropriate flip-flops (125 and 133) operate with proper setup and hold times. There are several options for implementing the clock phase selector 131. For instance, if the delay of the total clock path is predictable and within a small range, then a simple fixed value delay line can be implemented for the phase selector. This option has the advantage of being low cost. Alternatively, a coarse phase selector could be used to compare two local pixel clocks, 0 and 180 degrees, and pick the one that provides the best setup and hold time margins for the re-synchronization flip-flops. This method may be preferred for most applications. Yet another alternative

is to use a phase-locked-loop (PLL) to develop the correct timing for the resynchronization flip-flops, resulting in the best setup and hold time margins. The PLL could be a simple phase-only tracking circuit. This approach offers finer phase steps than the coarse phase selector.

FIGURE 2 is another schematic diagram of an alternative electronic circuit 200 for connecting a video data source to a video DAC. The alternative circuit 200 includes only those components used in the re-clocking scheme described above for addressing the problem of beat patterns. An external clock reference 207 provides a signal to a local clock generator 209, which in turn outputs a pixel clock signal 211 via a clock buffer 213. Clock logic circuitry 215 processes the pixel clock signal 211 and provides a processed pixel clock signal 217 to the video DAC circuit 205 as well as a video data source 219. The video data source 219 provides a video data signal 221 to the video DAC circuit 205 in sync with the processed pixel clock 217.

The video data source 203 can be either remote or local to the video DAC circuit 205. The pixel clock signal 211 and the processed pixel clock signal 217 are sensitive paths to interferences. If there are more circuits extending these signal paths, either inside or outside the block boundaries, those are also sensitive to interferences. For these reasons, the circuit 200 would be susceptible to beat patterns in the absence of the teachings of the present invention.

In this embodiment, the processed pixel clock signal 217 is coupled only to a first flip-flop 225 for latching the video data signal 221. The local clock generator 209 is coupled, via a clock phase selector 231, to the clock inputs of a second flip-flop 227 and an RGB DAC 229. In this configuration, the processed pixel clock 217 is used to clock the first flip-flop 225, but the local clock generator 209 is used for timing the second flip-flop 227 and the DAC 229. In this configuration, the processed pixel clock signal 217 is a buffered version (same frequency) of the pixel clock signal 211. As just mentioned, the clock feeding the second flip-flop 227 and the RGB DAC 229 is taken from the local clock generator 209. Because the connection is short and local, interference from other system clock sources should be insignificant. The second flip-flop 227, which again may contain several flip-flops, is re-clocked with the local "clean" timing, thus the output should be free of beat patterns. Note that the circuit

Docket No.: 08211/000S081-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hee Wong

Application No.: 09/864,561 Art Unit: 2674

Filed: May 23, 2001 Examiner: R. Laneau

For: METHOD AND APPARATUS FOR ADDRESSING BEAT PATTERNS IN AN INTEGRATED VIDEO DISPLAY SYSTEM

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated December 5, 2003 (Paper No. 6), please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Conclusion begins on page 8 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for clocking video data to reduce beat patterns, comprising:

receiving a video data signal having a predetermined pixel frequency based on an external clock reference, the video data signal being provided by video data signal circuitry; and

providing a local clock signal to re-clock the video data signal at a final stage of a video path between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference, thereby removing interfering influence of other clock signals on the predetermined pixel frequency.

2. (Original) The method of claim 1, wherein the video data signal is received within an integrated video display system.

3. (Original) The method of claim 1, wherein the video data signal is generated within an integrated video display system.

4. (Original) The method of claim 1, wherein the output circuitry comprises a digitalto-analog converter subcircuit.

5. (Original) The method of claim 4, wherein providing the local clock signal comprises latching the video data signal with at least one latching subcircuit clocked by the local clock signal.

6. (Original) The method of claim 5, wherein the latching subcircuit comprises at least one flip-flop configured to latch the video data signal through to the output circuitry, the flip-flop being clocked by the local clock signal.

7. (Currently Amended) An integrated video display system for providing a video signal having reduced beat patterns, comprising:

a video data circuit coupled to an output circuit through a latching circuit, the video data circuit being configured to provide a video data signal based on a pixel frequency, the pixel frequency being based on an external clock reference, the latching circuit being at a final stage of a video path between the video data signal circuit and the output circuit; and

a re-clocking circuit coupled to the latching circuit, the re-clocking circuit being configured to provide a local clock signal for re-clocking the video data signal through the latching circuit, wherein re-clocking the circuit is based on the external clock reference, and the video data signal is provided to the output circuit based on the local clock signal.

8. (Cancelled)

9. (Original) The integrated video display system of claim 7, wherein the latching circuit comprises at least one flip-flop configured to latch the video data signal through to the output circuit, the flip-flop being clocked by the local clock signal.

10. (Original) The integrated video display system of claim 9, wherein the flip-flop is part of a final stage for the video data signal prior to being coupled to the output circuit.

11. (Original) The integrated video display system of claim 7, wherein the output circuit comprises a digital-to-analog converter subcircuit.

12. (Original) The integrated video display system of claim 7, further comprising a selection circuit for selectively switching between conventionally clocking the video data signal based on the pixel frequency and re-clocking the video data signal based on the local clock signal.

13. (Currently Amended) An integrated video display system for providing a video signal having reduced beat patterns, comprising:

a video data source based on a predetermined pixel frequency;

an output circuit;

a conventional clocking circuit including a clock signal based on the predetermined pixel frequency;

a re-clocking circuit having a frequency based on a clock signal provided by a local clock generator; and

a select switch for selectively coupling the video data source to the output circuit based on either the conventional clocking circuit or the re-clocking circuit,

wherein interfering influence of other clock signals on the predetermined pixel frequency is removed if the re-clocking circuit is coupled a final stage of a video path between the video data source and the output circuit.

14. (Original) The integrated video display system of claim 13, wherein the predetermined pixel frequency is based on an external clock reference and wherein the local clock generator is based on the external clock reference.

15. (Original) The integrated video display system of claim 14, wherein the local clock generator provides a pixel clock signal to the video data source on which to base the predetermined pixel frequency.

16. (Original) The integrated video display system of claim 13, wherein the output circuit comprises a digital-to-analog converter subcircuit.

17. (Original) The integrated video display system of claim 13, wherein the re-clocking circuit comprises at least one latching subcircuit clocked by the local clock generator.

18. (Original) The integrated video display system of claim 17, wherein the latching subcircuit comprises at least one flip-flop configured to latch the video data source through to the output circuitry, the flip-flop being clocked by the local clock signal.

19. (Original) The integrated video display system of claim 18, wherein the latching subcircuit is coupled to the video data source and the output circuitry, and wherein the output circuitry comprises a digital-to-analog converter subcircuit.

20. (Original) The integrated video display system of claim 19, wherein the latching subcircuit is the final stage of a video data path between the video data source and the output circuitry.

Version With Markings To Show Changes Made

In the Specification:

The paragraph beginning at line 10 of page 6 has been amended as follows:

(Amended) The first operation mode (Scheme A) occurs when the scheme select switch 123 is in the "A" position. In that position, the processed pixel clock signal 11[1]7 is coupled to a first D flip-flop 125, a second D flip-flop 127, and to the RGB DAC 129. It will be appreciated that although only a single flip-flop and DAC may be shown in FIGURE 1, there may in fact be several D flip-flops and DACs, one per data line. In this configuration, the processed pixel clock 117 is used to latch the video data signal 121 through to the RGB DAC 129.

The paragraph beginning at line 23 of page 7 has been amended as follows:

(Amended) The clock phase selector 131 selects the proper clock phase for its two clock outputs so that the appropriate flip-flops (12[5]7 and 133) operate with proper setup and hold times. There are several options for implementing the clock phase selector 131. For instance, if the delay of the total clock path is predictable and within a small range, then a simple fixed value delay line can be implemented for the phase selector. This option has the advantage of being low cost. Alternatively, a coarse phase selector could be used to compare two local pixel clocks, 0 and 180 degrees, and pick the one that provides the best setup and hold time margins for the re-synchronization flip-flops. This method may be preferred for most applications. Yet another alternative is to use a phase-locked-loop (PLL) to develop the correct timing for the resynchronization flip-flops, resulting in the best setup and hold time margins. The PLL could be a simple phase-only tracking circuit. This approach offers finer phase steps than the coarse phase selector.

Application No. (if known): 09/864,561 Attorney Docket No.: 08211/000S081-US0

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